Listing of Claims:

1. (Previously Presented) A method of forming metal silicide on regions of a metal oxide semiconductor field effect transistor (MOSFET) device, comprising the steps of:

providing a MOSFET device on a semiconductor substrate comprised with a conductive gate structure on an underlying gate insulator layer and with a heavily doped source/drain region located in an area of said semiconductor substrate not covered by said conductive gate;

forming an interlayer material on said MOSFET device having a thickness less than 15 Angstroms;

forming a metal layer on said interlayer material;

performing an anneal procedure to form said metal silicide on said heavily doped source/drain region and on top surface of said conductive gate structure, while forming a layer comprised of said metal layer and said interlayer material on insulator spacers located on sides of said conductive structure; and

removing said layer comprised of said metal layer and said interlayer material from insulator spacers.

2. (Original) The method of claim 1, wherein said gate insulator layer is a silicon dioxide layer obtained via thermal oxidation procedures at a thickness between about 10 to 100 Angstroms, or said gate insulator layer can be a high k dielectric constant (high k) layer, with a dielectric constant greater than 4.

3. (Original) The method of claim 1, wherein said conductive gate structure is a polysilicon gate structure at a thickness between about 500 to 3000 Angstroms.

4. (Original) The method of claim 1, wherein said conductive gate structure is comprised with a width between about 0.01 to 10 um.

5. (Original) The method of claim 1, wherein said insulator spacers are comprised of silicon oxide or silicon nitride, at a thickness between about 200 to 1500 Angstroms.

6. (Original) The method of claim 1, wherein said heavily doped source/drain region is formed at a depth between about 200 to 2000 Angstroms in said semiconductor substrate.

7. (Original) The method of claim 1, wherein said interlayer material is titanium.

8. (Original) The method of claim 7, wherein said titanium layer is obtained at a thickness between about 10 to 15 Angstroms, via atomic layer deposition (ALD) procedures.

9. (Original) The method of claim 1, wherein said metal layer is a nickel layer obtained via physical vapor deposition procedures at a thickness between about 50 to 500 Angstroms.

10. (Original) The method of claim 1, wherein said anneal procedure is a rapid thermal anneal (RTA) procedure, performed at a temperature between about 250 to 700° C.

11. (Previously Presented) A method of forming nickel silicide on regions of a MOSFET device, comprising the steps of:

providing a MOSFET device on a semiconductor substrate comprised with a polysilicon gate structure on an underlying silicon dioxide gate insulator layer, with insulator spacers on sides of said polysilicon gate structure, and with a heavily doped source/drain region located in an area of said semiconductor substrate not covered by said polysilicon gate structure or by said insulator spacers;

forming a titanium interlayer on said MOSFET device having a thickness less than 15 Angstroms;

forming a nickel layer on said titanium interlayer;

performing a rapid thermal anneal (RTA) procedure to form said nickel silicide on said heavily doped source/drain region and on top surface of said polysilicon gate structure, while forming a nickel – titanium layer on said insulator spacers; and

selectively removing said nickel – titanium layer from insulator spacers.

12. (Original) The method of claim 11, wherein said silicon dioxide gas insulator is obtained via thermal oxidation procedures at a thickness between about 10 to 100 Angstroms.

13. (Original) The method of claim 11, wherein said polysilicon gate structure is comprised with a thickness between about 500 to 3000 Angstroms.

14. (Original) The method of claim 11, wherein said polysilicon gate structure is comprised with a width between about 0.01 to 10 um.

15. (Original) The method of claim 11, wherein said insulator spacers are comprised of silicon oxide or silicon nitride, at a thickness between about 200 to 1500 Angstroms.

16. (Original) The method of claim 11, wherein said heavily doped source/drain region is formed to a depth between about 200 to 2000 Angstroms in said semiconductor substrate.

17. (Currently Amended) The method of claim 11, wherein said titanium interlayer is obtained at a nearly uniform thickness ~~between about 10 to 15 Angstroms,~~ via atomic layer deposition (ALD) procedures.

18. (Original) The method of claim 11, wherein said nickel layer is obtained via physical vapor deposition procedures at a thickness between about 50 to 500 Angstroms.

19. (Previously Presented) The method of claim 11, wherein said RTA procedure is performed at a temperature between about 250 to 700°C.

20. (Original) A method of forming nickel silicide on regions of a MOSFET device featuring a titanium interlayer obtained via atomic layer depositions procedures, wherein said titanium interlayer is used to optimize nickel silicide formation, comprising the steps of:

providing a MOSFET device on a semiconductor substrate comprised with a polysilicon gate structure on an underlying silicon dioxide gate insulator layer, with insulator spacers on sides of said polysilicon gate structure, and with a heavily doped source/drain region located in an area of said semiconductor substrate not covered by said polysilicon gate structure or by said insulator spacers;

performing said atomic layer deposition procedure to form said titanium interlayer on said MOSFET device, with said titanium interlayer formed at a thickness between about 10 to 15 Angstroms;

forming a nickel layer on said titanium interlayer;

performing said rapid thermal anneal (RTA) procedure to form said nickel silicide on said heavily doped source/drain region and on top surface of said polysilicon gate structure, while forming a nickel – titanium layer on said insulator spacers; and

selectively removing said nickel – titanium layer from insulator spacers.

21. (Original) The method of claim 20, wherein said silicon dioxide gate insulator layer is obtained via thermal oxidation procedures to a thickness between about 10 to 100 Angstroms.

22. (Original) The method of claim 20, wherein said polysilicon gate structure is comprised with a thickness between about 500 to 3000 Angstroms.

23. (Original) The method of claim 20, wherein said polysilicon gate structure is comprised with a width between about 0.01 to 10 um.

24. (Original) The method of claim 20, wherein said insulator spacers are comprised of silicon oxide or silicon nitride, at a thickness of between about 200 to 1500 Angstroms.

25. (Original) The method of claim 20, wherein said heavily doped source/drain region is formed to a depth between about 200 to 2000 Angstroms in said semiconductor substrate.

26. (Original) The method of claim 20, wherein said nickel layer is obtained via vapor deposition procedures at a thickness between about 50 to 500 Angstroms.

27. (Original) The method of claim 20, wherein said RTA procedure is performed at a temperature between 250 to 700°C, with a preferred temperature between about 300 to 450°C.

28. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate;

a metal oxide semiconductor field effect transistor (MOSFET) device formed in the substrate, comprising a conductive gate structure on an underlying gate insulator layer with a heavily doped source/drain region; and

a nickel silicide layer over the MOSFET, the nickel silicide layer formed by annealing a nickel layer adjacent a single titanium layer, the single titanium layer having a near uniform thickness less than about 15 Angstroms.

29. (Previously Presented) The semiconductor device of Claim 28, wherein the thickness of the titanium layer is between about 10 - 15 Angstroms.

30. (Previously Presented) The semiconductor device of Claim 28, wherein the titanium layer is formed by atomic layer deposition.